

JCS-4 U.S. PTO
09/496471



Class	Subclass	ISSUE CLASSIFICATION

PATENT NUMBER

U.S. UTILITY Patent Application

KW O.I.P.E. SCANNED _____ Q.A. <u>anw</u>	PATENT DATE
---	-------------

APPLICATION NO. 09/496421	CONT/PRIOR YES	CLASS 257	SUBCLASS 202	ART UNIT 2815	EXAMINER <i>LEG</i> <i>W. D. SP</i>
------------------------------	-------------------	--------------	-----------------	------------------	---

APPLICANTS

Ritsuko Iwasaki

三

Semiconductor device having an improved layout pattern of pair transistors

PTO-2040
12/99

ISSUING CLASSIFICATION

TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.				-NOTICE OF ALLOWANCE MAILED	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent No. _____ _____				ISSUE FEE	
<input type="checkbox"/> The terminal _____ months of the term of this patent has been disclaimed.				Amount Due	Date Paid
				ISSUE BATCH NUMBER	

WARNING:

WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 360. Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.

Form PTO-436A
(Rev. 6/99)

FILED WITH: DISK (CRF) FICHE CD-ROM
(Attached in pocket on right inside flap)